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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/055,088	01/22/2002	Arman Sagatelian	HPLA.006US0	8090

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EXAMINER
BRITT, CYNTHIA H

ART UNIT	PAPER NUMBER
2133	

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DATE MAILED: 09/08/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/055,088	SAGATELIAN ET AL.	
	Examiner	Art Unit	
	Cynthia Britt	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-20 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-20 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 22 January 2002 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 8/29/03.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-20 are presented for examination.

Information Disclosure Statement

The information disclosure statement (IDS), submitted on August 29, 2003 has been considered by the examiner. Form 1449 has been signed and returned with this office action.

Drawings

The drawings were received on January 22, 2002. These drawings are acceptable.

Claim Rejections - 35 USC § 102

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1,2 11, 12, and 20, are rejected under 35 U.S.C. 102(e) as being anticipated by Gangl et al. U.S. Patent No. 6,557,132.

As per claims 1, 11 and 20, Gangl et al. teach the claimed method and apparatus for determining common failure modes of an integrated circuit device under test is disclosed. In an exemplary embodiment of the invention, a test pattern is applied to a series of inputs of the device under test. A set of output data generated by the device

under test is then compared to a set of expected data, with the set of output data being generated by the device under test in response to the test pattern. It is then determined whether the set of output data has passed the test, with the set of output data passing the test if the set of output data matches the set of expected data. If the set of output data has not passed the test, then it is determined whether an output signature corresponding to the set of output data matches a previously stored output signature. Fail data corresponding to the output signature is then stored if the output signature matches a previously stored output signature. (Abstract, column 2 lines 1-20)

As per claims 2, and 12, Gangl et al. teach that by using the signature generation capability built into the tester, a comparison is performed of only the unique fail signatures generated without the use of complicated pattern recognition processes. Post-processing of the fail data is therefore greatly simplified, since the technique for identifying common fail modes involves looking for repeating values generated by DUT signatures as opposed to all of the vector data represented by the signatures. (Column 3 lines 56-67)

As per claims 9, 10, and 18, Gangl et al. teach if the device under test fails, then the fail signature is automatically stored. This process is repeated until all devices have been tested. Once all devices have been tested, a review process takes place. Each failed device has its signature reviewed to see whether it is unique with respect to the signatures of other failed devices. If a device is found to have a "repeat" fail signature, then that device is retested and its fail data collected (assuming the device exhibits a consistent fail signature when retested). After all failed devices have had their

signatures reviewed, the method comes to an end. By gathering data from the repeating signatures of failed test devices, a diagnosis as to the possible failure cause(s) may be undertaken. Once again, it has been shown that a comparison of signatures to check for repeat fail signatures rather than comparing entire vector states results in faster identification of common mode failures. Because the time required to generate and capture such information is relatively small, larger sample sizes can be generated, thereby allowing extra data to be captured with less overhead for data collection. Furthermore, the above disclosed embodiments of the invention are applicable to several different types of testing modes including, but not limited to Logic Built In Self Test (LBIST), Array Built In Self Test (ABIST), Scan Chain, functional, and stuck-fault. (Figure 3, column 4 lines 1-30)

As per claim 19, Gangl et al. teach the method can include embodiments in the form of computer-implemented processes and apparatuses for practicing those processes. The present invention can also include embodiments in the form of computer program code containing instructions embodied in tangible media, such as floppy diskettes, CD-ROMs, hard drives, or any other computer-readable storage medium, wherein, when the computer program code is loaded into and executed by a computer, the computer becomes an apparatus for practicing the invention. This can also include embodiments in the form of computer program code, for example, whether stored in a storage medium, loaded into and/or executed by a computer, or transmitted over some transmission medium, such as over electrical wiring or cabling, through fiber

optics, or via electromagnetic radiation, wherein, when the computer program code is loaded into and executed by a computer, the computer becomes an apparatus for practicing the method. When implemented on a general-purpose microprocessor, the computer program code segments configure the microprocessor to create specific logic circuits. (Column 4 lines 31-51)

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein

were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 3-9 and 13-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gangl et al. U.S. Patent No. 6,557,132 in view of "*The Value of Electrical Bitmap Results from Embedded Memory Arrays for Rapid Yield Learning*" Segal et al. Digest of Papers, 2nd IEEE Latin American Test Workshop LATW2001, pp. 266-272, Feb. 2001.

As per claims, 3-5 and 13-15, Gangl et al. substantially teach the claimed method and apparatus for determining common failure modes of an integrated circuit device under test is disclosed. In an exemplary embodiment of the invention, a test pattern is applied to a series of inputs of the device under test. A set of output data generated by the device under test is then compared to a set of expected data, with the set of output data being generated by the device under test in response to the test pattern. It is then determined whether the set of output data has passed the test, with the set of output data passing the test if the set of output data matches the set of expected data. If the set of output data has not passed the test, then it is determined whether an output signature corresponding to the set of output data matches a previously stored output signature. Fail data corresponding to the output signature is then stored if the output signature matches a previously stored output signature. (Abstract, column 2 lines 1-20)

Not explicitly disclosed is the use of the bitmap data and the logic OR combining.

However, in an analogous art, Segal et al. teach a system and method of using bitmap signature fail data to determine fault sources for device failure. Where there may be more than one candidate for the defect type causing the failure. However, with results from multiple bitmaps from the same lot, one can look at the distribution of signatures and compare that to the distribution of signatures predicted for each defect type. Each defect type has a unique distribution of failing bitmap signatures associated with it. The actual electrical results represent a linear combination of these, which can be analyzed to find the contribution of the individual defect types. Analysis of electrical bitmap results from embedded memories can provide significant value for yield diagnosis and failure analysis. The bitmap results can be correlated to in-line defects or compared to falling signatures predicted by realistic fault extraction. As per the use of a logical OR to combine the bits, the examiner would like to point out that the use of logic OR gates to combine or add is well known and commonly used in this art. The resulting understanding of physical failure mechanisms and yield modeling applies to the logic blocks on the same chip, as well as to other designs running in the same fabrication facility (page 6 paragraphs 2 and 3). Therefore, it would have been obvious to a person having ordinary skill in the art at the time this invention was made to have used the method and apparatus for determining common failure modes of an integrated circuit device under test taught by Gangl et al. with the bitmap signature fail data to determine fault sources for device failure taught by Segal et al. This would have been obvious as

suggested by Gangl et al. in order to reduce test time and ascertain the specific failure mode of a device (column 1 lines 40-49).

As per claims, 6-8 and 16-16, Gangl et al. substantially teach the claimed method and apparatus for determining common failure modes of an integrated circuit device under test is disclosed. In an exemplary embodiment of the invention, a test pattern is applied to a series of inputs of the device under test. A set of output data generated by the device under test is then compared to a set of expected data, with the set of output data being generated by the device under test in response to the test pattern. It is then determined whether the set of output data has passed the test, with the set of output data passing the test if the set of output data matches the set of expected data. If the set of output data has not passed the test, then it is determined whether an output signature corresponding to the set of output data matches a previously stored output signature. Fail data corresponding to the output signature is then stored if the output signature matches a previously stored output signature. (Abstract, column 2 lines 1-20) Not explicitly disclosed is the use of the bitmap data and the logic OR combining.

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with it. The actual electrical results represent a linear combination of these, which can be analyzed to find the contribution of the individual defect types. Analysis of electrical bitmap results from embedded memories can provide significant value for yield diagnosis and failure analysis. The bitmap results can be correlated to in-line defects or compared to falling signatures predicted by realistic fault extraction. As per the use of a logical OR to combine the bits, the examiner would like to point out that the use of logic OR gates to combine or add is well known and commonly used in this art. The resulting understanding of physical failure mechanisms and yield modeling applies to the logic blocks on the same chip, as well as to other designs running in the same fabrication facility (page 6 paragraphs 2 and 3). Therefore, it would have been obvious to a person having ordinary skill in the art at the time this invention was made to have used the method and apparatus for determining common failure modes of an integrated circuit device under test taught by Gangl et al. with the bitmap signature fail data to determine fault sources for device failure taught by Segal et al. This would have been obvious as suggested by Gangl et al. in order to reduce test time and ascertain the specific failure mode of a device (column 1 lines 40-49).

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

U.S. Patent No. 5,930,270 Forlenza et al.

This patent teaches a system and method for diagnosing the faults of an electronic device by running a series of tests, identifying the tests where the electronic device failed, without having to check the results of each test, storing information generated during only the tests where the electronic device failed, and using the information to diagnose the faults in the electronic device. The test results are accumulated into a Multiple Input Shift Register (MISR), which need not be examined after each test to determine which tests the device failed. The problem of a failure during one test manifesting into the MISR during subsequent tests is handled by predicting the effect of the failure on the MISR during subsequent tests.

U.S. Patent No. 5,727,000 Pizzica

This patent teaches test equipment and test methods employing signature analysis to achieve fault isolation of parts contained in digital modules. Fault free signatures of a digital module are stored in a lookup table that are derived from physical measurement or simulation of all parts. All of the parts in the functional digital module are shorted and opened (either physically or by simulation) and each of their resulting faulty signatures are recorded in a storage device. Each signature with its corresponding faulty part is stored in the lookup table or memory. Test input signals are then applied to a tested digital module, and outputs of all parts thereof are applied to masking circuitry which allows sequential selective masking of all parts but one, for each part on the tested digital module. Outputs of the masking circuitry are applied to a multiple input shift register signal analyzer that performs pass/fail signature analysis

using the applied signals. When a failure occurs during testing of the tested digital module, comparator circuitry is used to find a corresponding signature match to the stored faulty signatures. A message is then sent as an output from the comparator circuitry identifying the failed part so that the tested digital module can be repaired.

U.S. Patent No. 4,503,536 Panzer

This patent teaches a system for testing digital circuit units at the design speed of the circuit. A first memory stores a minimized set of optimum generated predetermined test patterns for application to a unit under test. A second memory stores expected signature patterns corresponding to signature patterns that are derived from the unit under test in response to the predetermined test patterns when the unit under test is functioning properly. A signature analyzer derives signature patterns from a unit under test in response to the application of the test patterns to the unit. A comparator compares the derived signature patterns with the expected signature patterns and provides an indication of the results of the comparison. A clock provides a clock signal having a pulse rate that corresponds to the design speed of the unit under test; and a sequential counter responds to said clock signal by providing a sequential count to the first memory for addressing the first memory at storage positions therein having addresses corresponding to the sequential count to cause the predetermined test patterns to be read from the first memory and applied to the unit at a speed that corresponds to the design speed of the unit under test. The testing system further

includes a backtracing system for enabling determination of the location of faults in the unit under test.

"Predicting Failing Bitmap Signatures for Memory Arrays with Critical Area Analysis" Segal et al. Advanced Semiconductor Manufacturing Conference and Workshop, 1999 IEEE/SEMI Publication Date: 8-10 Sept. 1999 pages: 178 - 182 Inspec Accession Number: 6512794

This paper teaches using in-line defect data, critical area analysis of cell layout, and a rule-based algorithm to associate critical areas with electrical faults, we can predict failing bitmap signatures and their frequencies for any memory circuit. The technique is demonstrated using a 0.25 μm SRAM technology. Results can be used for test optimization, redundancy planning, yield prediction, and determining process steps responsible for yield loss.

"*Early Error Detection in Systems-on-Chip for Fault-Tolerance and At-Speed Debugging*" by Sogomonyan et al. 19th IEEE Proceedings on VLSI Test Symposium Publication Date: 29 April-3 May 2001 pages184 - 189 Inspec Accession Number: 7023720

This paper teaches a method for the design of duplex fault-tolerant systems with early error detection and high availability. All the scannable memory elements (flip-flops) of the duplicated system are implemented as multimode memory elements according to Singh et al. (1999), thus allowing during normal operation the accumulation of a

signature of its states in its scan-paths. By continuously comparing a 1-bit sequence of the compacted scan-out outputs of the accumulated signatures of the duplicated systems an error can be already detected and a recovery procedure started before an erroneous result appears at the system outputs when a computations is completed. The accumulation of a signature during normal operation can also be used for debugging at-speed. For this application the system need not be duplicated

"Efficient Implementation of Multiple On-Chip Signature Checking" Abdulla et al. 10th International Conference on VLSI Design, Publication Date: 4-7 Jan. 1997 pages297 - 302 Inspec Accession Number: 5565767

This paper teaches detection latency in a BIST scheme is the delay between the time instant at which a faulty response appears and the time instant at which the fault is detected. Conventional BILBO-BIST schemes suffer from long detection latency since it is not until the signatures are scanned out and compared off-chip, that a fault becomes apparent. Aliasing, which is a fallout of long detection latency, is a serious problem. A proposed improved BIST architecture, which supports on-chip comparison of multiple signatures to minimize the probability of aliasing and total test time. Also quantified the aliasing probability of the "Multiple On-chip Signature Comparison scheme" (MOSC) scheme proposed. In this paper, an efficient implementation of the MOSC test architecture and report results on several benchmark circuits is described.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Cynthia Britt whose telephone number is 703-308-2391. The examiner can normally be reached on Monday - Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on 703-305-9595. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Cynthia Britt
Examiner
Art Unit 2133